In the Claims:

Please amend the claims as follows:

1. (Original) A SOI-type semiconductor substrate comprising at least a buried insulating cavity formed according to the following steps:

form on said semiconductor substrate a plurality of trenches,

form a surface layer on said semiconductor substrate in order to close superficially said plurality of trenches forming, in the meantime, said at least one cavity buried in correspondence with the surface-distal end of said trenches;

form a first semiconductor material layer on said surface layer with the same concentration as said semiconductor substrate wherein at least a trench is formed which is in communication with said at least one buried cavity.

2. (Original) A semiconductor substrate according to claim 1 wherein said surface layer is formed through an annealing step in a non-oxidizing atmosphere on all said semiconductor substrate.

3. (Original) A semiconductor substrate according to claim 1 wherein said surface layer is formed by means of a semiconductor material surface layer formed in the substrate.

4. (Original) A semiconductor substrate according to claim 3 wherein said semiconductor material surface layer is formed on the substrate through epitaxy.

5. (Original) A semiconductor substrate according to claim 1 wherein said first semiconductor material layer is formed through epitaxy.

6. (Original) A semiconductor substrate according to claim 1 wherein portions of said semiconductor substrate around said at least one buried cavity are of a porous silicon layer.

7. (Original) A semiconductor substrate according to claim 5 wherein said porous silicon layer is oxidized forming a dielectric layer between said surface layer and a lower semiconductor substrate portion.

8. (Original) A semiconductor substrate according to claim 7 wherein said porous silicon layer is removed to form a second buried cavity of a wider width than said at least one starting buried cavity.

9. (Currently Amended) A suspended membrane formed on a semiconductor substrate of a first type of concentration and comprising at least a buried insulating cavity formed through the following steps:

form on said semiconductor substrate a plurality of trenches,

perform an annealing step in a non-oxidizing atmosphere on all said semiconductor substrate up to form a surface layer on said semiconductor substrate in order to close superficially said plurality of trenches forming in the meantime said at least one buried cavity in correspondence with the surface-distal end of said trenches, said surface layer forming said membrane, and forming a first semiconductor material layer on the surface layer with at least one trench being formed in the first semiconductor material layer which intersects with at least one of the buried cavities.

10. (Original) A suspended membrane formed on a semiconductor substrate according to claim 9 wherein a first semiconductor material layer is formed on said surface layer with different concentration with respect to said semiconductor substrate.

11. (Original) A suspended membrane formed on a semiconductor substrate according to claim 10 wherein said first layer is an epitaxial layer.

12. (Original) A suspended membrane formed on a semiconductor substrate according to claim 11 wherein a portion of said semiconductor substrate located in correspondence with said at least one buried cavity is a porous silicon layer.

13. (Original) A microphone integrated on a semiconductor substrate wherein it comprises a membrane formed according to claim 9.

14. (Currently Amended) A MOSFET transistor integrated on a semiconductor substrate of a first type of concentration and comprising at least one buried insulating cavity formed through the following steps:

form on said semiconductor substrate a plurality of trenches,

perform an annealing step in a non-oxidizing atmosphere on all said semiconductor substrate up to form a surface layer on said semiconductor substrate in order to close superficially said plurality of trenches, and forming in the meantime said at least one buried cavity in correspondence with the surface-distal end of said trenches, and forming a first semiconductor material layer on the surface layer with at least one trench being formed in the first semiconductor material layer which is in communication with said at least one buried cavity, and said at least one buried insulating cavity forming at least part of the channel region of said MOSFET transistor.

15. (Original) A MOSFET transistor integrated on a semiconductor substrate according to claim 14 wherein a first layer is formed on said surface layer with the same concentration of said semiconductor substrate.

16. (Original) A MOSFET transistor integrated on a semiconductor substrate according to claim 15 wherein said first layer is formed through epitaxy.

17. (Original) A MOSFET transistor integrated on a semiconductor substrate according to claim 14 wherein a portion of said semiconductor substrate located in correspondence with said at least one buried cavity is a porous silicon layer.

18. (Withdrawn) A method for manufacturing a semiconductor substrate of a first type of concentration and comprising at least one buried insulating cavity, comprising the following steps:

form on said semiconductor substrate a plurality of trenches,

form a surface layer on said semiconductor substrate in order to superficially close said plurality of trenches forming in the meantime said at least one buried cavity in correspondence with the surface-distal end of said trenches.

19. (Withdrawn) A method for manufacturing a semiconductor substrate according to claim 18 wherein said surface layer is formed through an annealing step in a non-oxidizing atmosphere on all said semiconductor substrate.

20. (Withdrawn) A method for manufacturing a semiconductor substrate according to claim 18 wherein said surface layer is formed through a semiconductor material surface layer formed on the substrate.

21. (Withdrawn) A method for manufacturing a semiconductor substrate according to claim 18 wherein said semiconductor material surface layer is formed on the substrate through epitaxy.

22. (Withdrawn) A method for manufacturing a semiconductor substrate according to claim 18 wherein it comprises the following steps:

form a first layer on said surface layer having the same concentration as said semiconductor substrate.

23. (Withdrawn) A method for manufacturing a semiconductor substrate according to claim 20 wherein at least one trench being in communication with said at least one buried cavity is formed in said first layer.

24. (Withdrawn) A method for manufacturing a semiconductor substrate according to claim 18 wherein said semiconductor substrate is subjected to an electroerosive process to turn a portion of said semiconductor substrate located in correspondence with said at least one buried cavity into a porous silicon layer.

25. (Withdrawn) A method for manufacturing a semiconductor substrate according to claim 18 wherein said porous silicon layer is subjected to an oxidizing process

to form a dielectric layer between said surface layer and a semiconductor substrate lower portion.

26. (Withdrawn) A method for manufacturing a semiconductor substrate according to claim 24 wherein said porous silicon layer is removed to form a second buried cavity with a wider width than said at least one starting buried cavity.

27. (Withdrawn) A method for manufacturing a semiconductor substrate according to claim 18 wherein said plurality of trenches is formed by grooves being parallel to each other in the substrate.

28. (Withdrawn) A method for manufacturing a semiconductor substrate according to claim 18 wherein said plurality of trenches are formed by cylindrically-developing openings in the substrate.

29. (Withdrawn) A method, comprising:
forming openings in a substrate; and
closing the openings to form at least one cavity within the substrate.

30. (Withdrawn) The method of claim 29 wherein forming openings comprises forming trenches in the substrate.

31. (Withdrawn) The method of claim 29 wherein forming openings comprises forming rows of cylindrical openings in the substrate.

32. (Withdrawn) The method of claim 29 wherein closing the openings comprises heating the substrate.

33. (Withdrawn) The method of claim 29 wherein closing the openings comprises heating the substrate to approximately 1000° C – 1300° C for at least ten minutes in a non-oxidizing environment.

34. (Withdrawn) The method of claim 29 wherein closing the openings comprises forming a layer on the substrate to cover the openings.

35. (Withdrawn) The method of claim 29, further comprising forming a buried dielectric layer by converting a wall of the cavity into a dielectric material.

36. (Withdrawn) The method of claim 29, further comprising:

forming an opening to the cavity; and

forming a buried dielectric layer by converting a wall of the cavity into dielectric material via the opening.

37. (Withdrawn) The method of claim 29, further comprising:

converting a wall of the cavity into porous silicon; and

forming a buried dielectric layer by oxidizing the porous silicon.

38. (Withdrawn) The method of claim 29, further comprising enlarging the cavity.

39. (Withdrawn) The method of claim 29, further comprising:

converting a wall of the cavity into a material that is different than the material from which the substrate is formed; and

enlarging the cavity by removing the material

40. (Withdrawn) The method of claim 29, further comprising:

converting a wall of the cavity into porous silicon; and

enlarging the cavity by removing the porous silicon.

41. (Currently Amended) A semiconductor structure, comprising:

a first portion of a semiconductor substrate;

a cavity disposed in the first portion of the semiconductor substrate;

a second portion of the semiconductor substrate disposed over the cavity;

at least one trench formed in the second portion of the semiconductor substrate, each trench adjoining the cavity; and

a device disposed in the second portion of the semiconductor substrate.

42. (Original) The semiconductor structure of claim 41 wherein the device comprises transistor.

43. (Original) The semiconductor structure of claim 41 wherein the device comprises a transducer.

44. (Original) The semiconductor structure of claim 41 wherein the device comprises a microphone.

45. (Original) A semiconductor structure, comprising:

a first portion of a semiconductor substrate;

a dielectric layer disposed on the first portion of the semiconductor substrate and having a remnant of a cavity;

a second portion of the semiconductor substrate disposed on the dielectric layer and being electrically insulated from the first portion of the semiconductor substrate; and

a semiconductor device disposed in the second portion of the semiconductor substrate.